PRODUCT SPECIFICATION

3.5” a-Si TFT LCD MODULE
MODEL: T063-A0 Ver:1.1

ROHS

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER’S APPROVAL	
CUSTOMER :	
SIGNATURE:	DATE:

APPROVED BY	PM REVIEWED	PD REVIEWED	PREPARED BY

Revision History

Revision	Date	Originator	Detail	Remarks
1.0	2011-10-18		Initial Release	
1.1	2011-11-3		Update the drawing	

Table of Contents

1. General Description

The specification is a transmissive type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs and a backlight unit.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	3.5”	
LCD type	α-Si TFT	
Display Mode	TN /Transmissive /Normally white	
Resolution	320 RGB x 240	Pixels
View Direction	12 O’clock	Best Image
Module Outline	76.9(H) x 63.9(V) x 3.15(T) (Note1)	mm
Active Area	70.08(H) x 52.56(V)	mm
Pixel Size	219(H) x219(V)	um
Pixel Arrangement	Stripe	
Polarizer Surface Treatment	Normal	
Display Colors	16M	
Interface	24-bit RGB Interface	
Driver IC	NT39016D	-
Operating Temperature	-20～70	ºC
Storage Temperature	-30～80	ºC
Weight	21	g

Note 1: Exclusive hooks, posts , FFC/FPC tail etc.

3. Absolute Maximum Ratings

V_{SS}=0V, Ta=25ºC

Item		Symbol	Min.	Max.	Unit
Supply Voltage	Logic	VDD	-0.5	5	V
	Analog	VCI	-0.5	7.5	V
Power supply voltage		DDVDH-AGND	-0.3	5.5	
Power supply voltage		VGH-VGL	-0.3	25	
LED forward voltage		V_F	-	3.5	One LED
LED forward current		I_F	-	20	One LED
Storage temperature		T_{stg}	-30	+80	ºC
Operating temperature		T_{op}	-20	+70	ºC

Note 1: If Ta below 50ºC, the maximal humidity is 90%RH, if Ta over 50ºC, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Logic	VDD	3.0	3.3	3.6	V
	Analog	VCI	4.8	5.0	5.2	V
Logic Low input voltage		V_{IL}	0	-	0.2*VDD	V
Logic High input voltage		V_{IH}	0.8*I VDD	-	VDD	V
Logic Low output voltage		V_{OL}	0	-	VSS+0.4	V
Logic High output voltage		V_{OH}	VDD-0.4	-	VDD	V
Current Consumption All White	Logic	$I_{CC+}I_{IN}$	-	12	-	mA
	Analog					
Current Consumption All Black	Logic	I_{CC+} I_{IN}	-	12	-	mA
	Analog					
Current Consumption RGB	Logic	I_{CC+} I_{IN}	-	12	-	mA
	Analog					
Current Consumption Sleep	Logic	I_{CC+} I_{IN}	-	-	100	uA
	Analog					

5. Backlight Characteristic

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Voltage	V_F	Ta=25 ºC, I_F=15mA/LED	18.0	19.2	20.4	V
Forward Current	I_F	Ta=25 ºC, V_F=3.2V/LED	-	15	20	mA
Reverse Voltage	V_R	-	-	-	-	V
Reverse current	I_R		-	-	-	uA
Power dissipation	Pd		-	288	408	mW
Uniformity	Avg		80	85	-	%
Drive method	Constant current					
LED Configuration	6 White LEDs in series					

6. Optical Characteristics

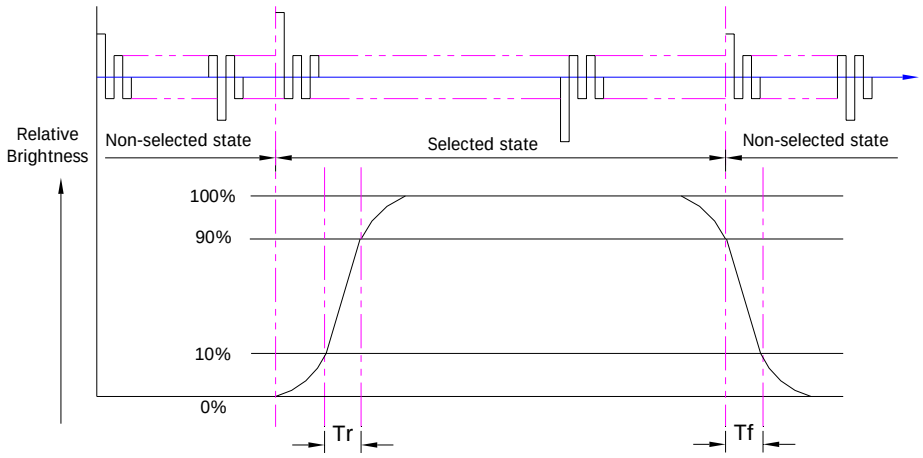
6.1. Optical Characteristics

Ta=25ºC, V_{DD} =3.3V, TN LC+ Polarizer

	Item		Symbol	Condition	Specification			Unit
					Min.	Typ.	Max.	
Backlight On (Transmissive Mode)	Transmittance(See 6.6)		T%	Normally viewing angle θx = φy =0º	6.9	7.5	-	%
	Luminance on TFT(I_f =15mA/LED)		Lv		190	240	-	cd/m²
	Contrast ratio(See 6.3)		CR		-	350	-	
	Response time (See 6.2)		TR+TF		-	35	60	ms
	Chromaticity Transmissive (See 6.5)	Red	XR		0.586	0.636	0.686	
			YR		0.300	0.350	0.400	
		Green	XG		0.261	0.311	0.361	
			YG		0.501	0.551	0.601	
		Blue	XB		0.084	0.134	0.184	
			YB		0.101	0.151	0.201	
		White	XW		0.261	0.311	0.361	
			YW		0.300	0.350	0.400	
	Viewing Angle (See 6.4)	Horizontal	θx+	Center CR≥10	50	60	-	Deg.
			θx-		50	60	-	
		Vertical	φy+		50	60	-	
			φy-		30	40	-	
	NTSC Ratio(Gamut)				-	50	-	%

6.2. Definition of Response Time

6.2.1. Normally Black Type (Negative)

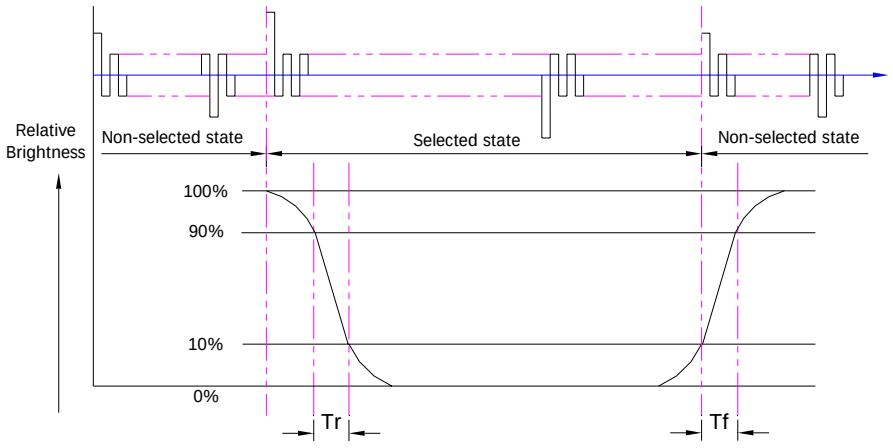


Tr is the time it takes to change form non-selected stage with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note : Measuring machine: LCD-5100

6.2.2. Normally White Type (Positive)



Tr is the time it takes to change form non-selected stage with relative luminance 90% to selected state with relative luminance 10%;
Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;
Note : Measuring machine: LCD-5100 or EQUI

6.3. Definition of Contrast Ratio

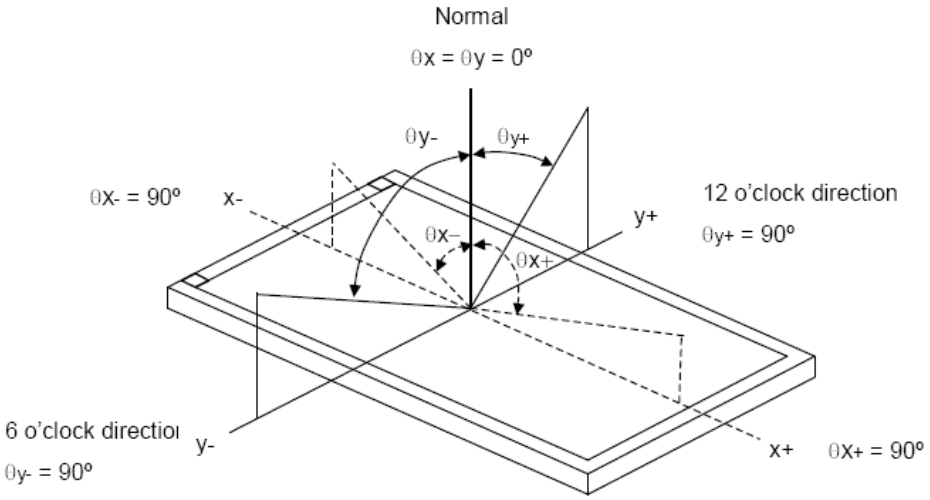
Contrast is measured perpendicular to display surface in reflective and transmissive mode.

The measurement condition is:

Measuring Equipment	Eldim or Euivelent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

6.4. Definition of Viewing Angles



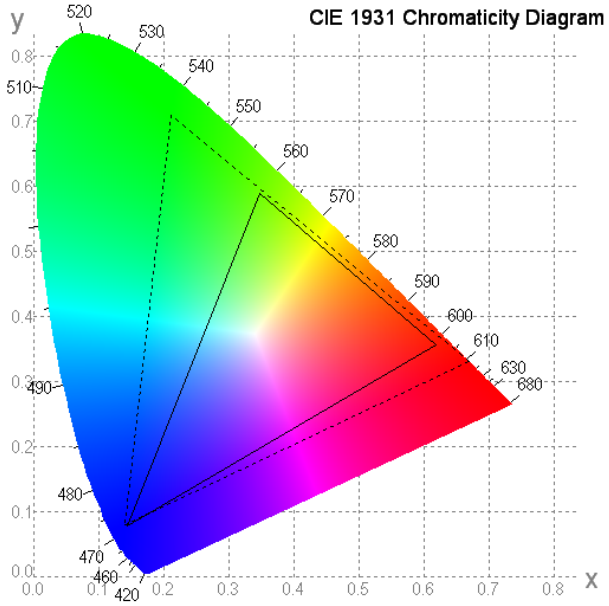
Measuring machine: LCD-5100 or EQUI

6.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



6.6. Definition of Surface Luminance, Uniformity and Transmittance

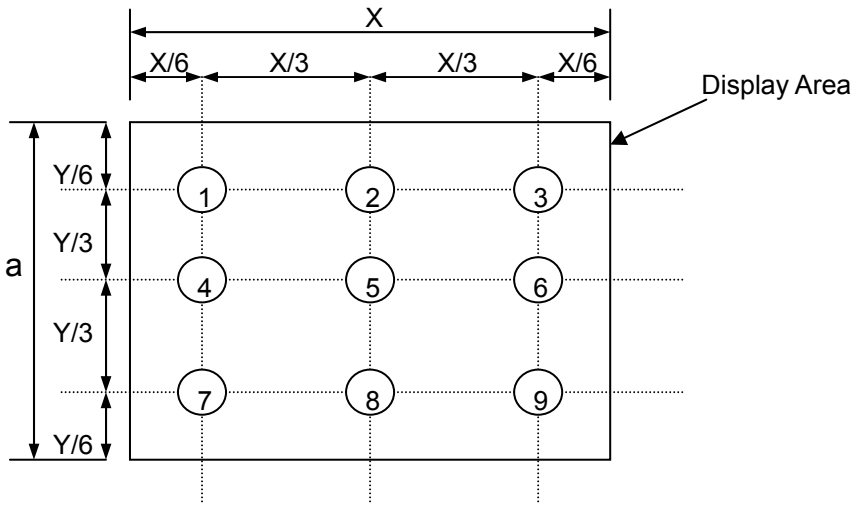
Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

6.6.1. Surface Luminance: L_V = average (L_{P1}:L_{P9})

6.6.2. Uniformity = Minimal (L_{P1}:L_{P9}) / Maximal (L_{P1}:L_{P9}) * 100%

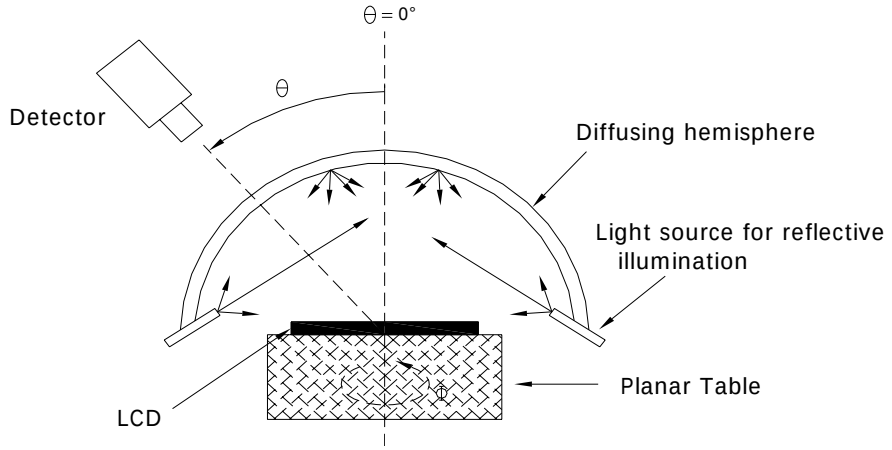
6.6.3. Transmittance = L_V on LCD / L_V on Backlight * 100%

Note : Measuring machine: BM-7

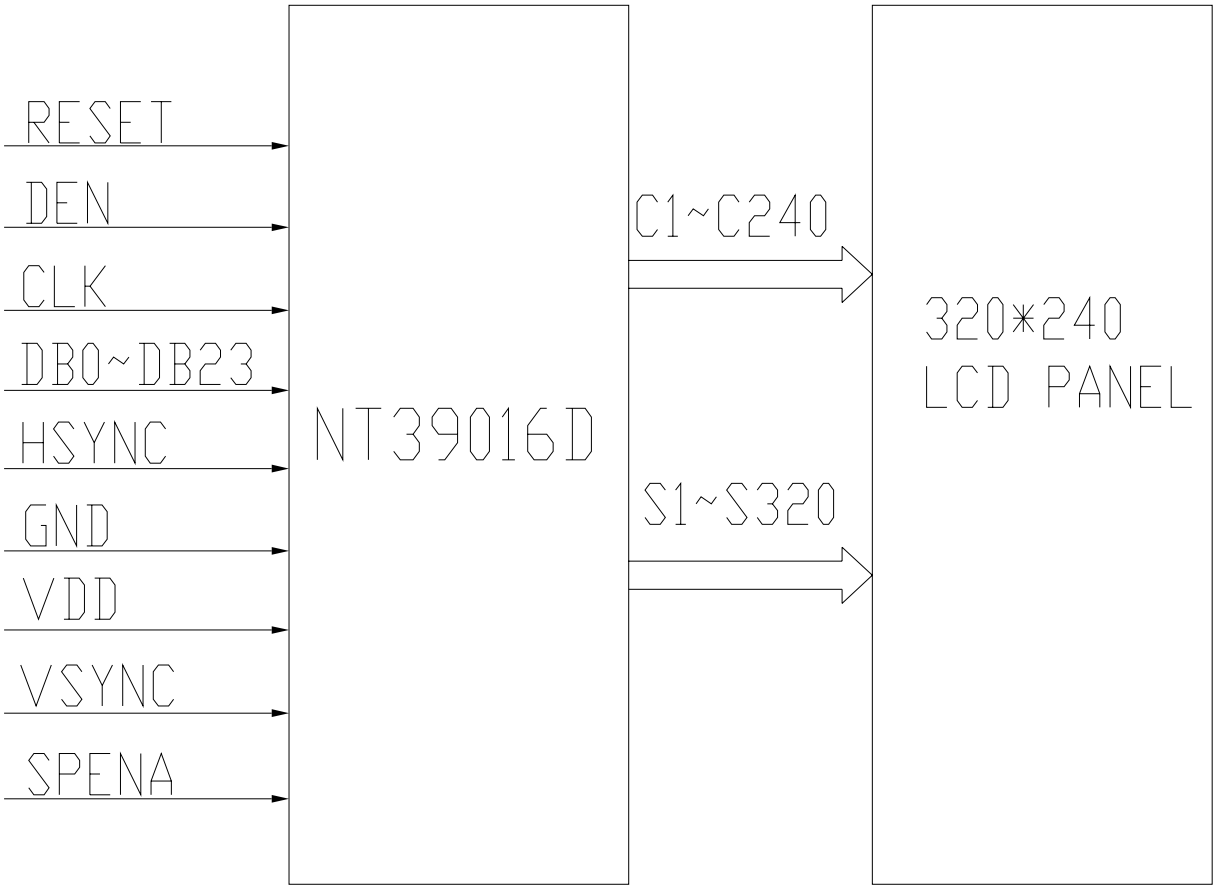


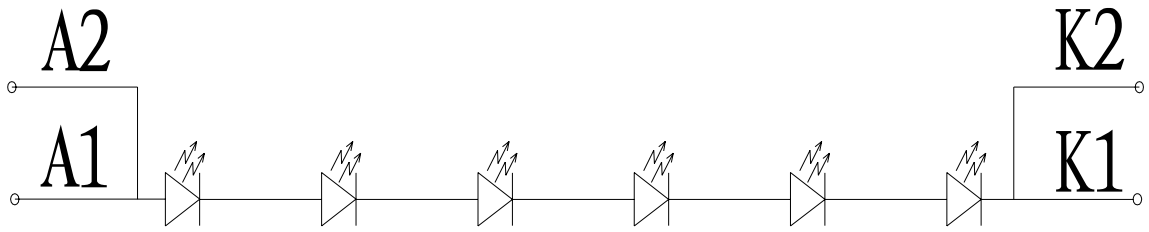
6.7. Definition of Reflectivity

To measure the reflectivity, the detector should be aligned to the normal direction of the LCD surface corresponding azimuthally angle θ=0°



7. Block Diagram and Power Supply





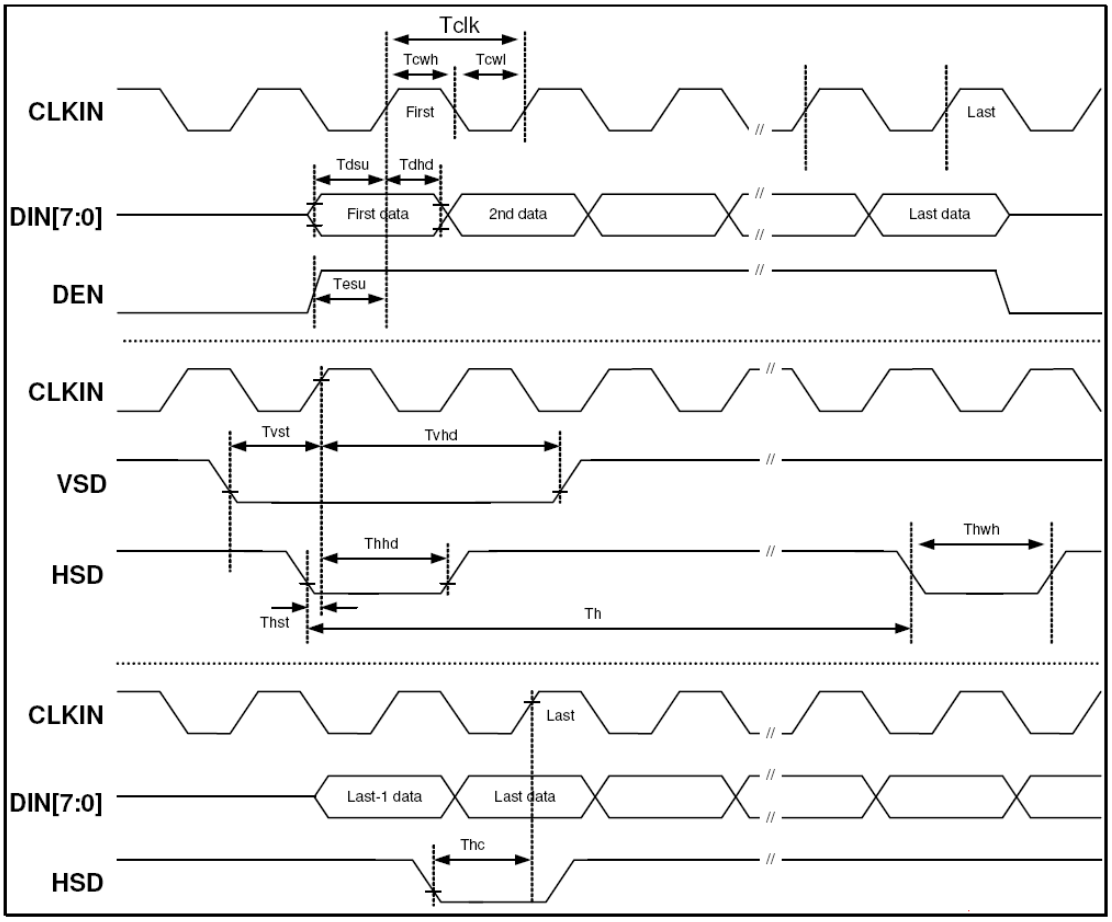
8. Interface Pins Definition

No.	Symbol	Function	Remark
1	LED_ K	LED cathode	
2	LED_ K	LED cathode	
3	LED_ A	LED anode	
4	LED_ A	LED anode	
5	NC	No connect	
6	NC	No connect	
7	NC	No connect	
8	RESET	Reset signal, Low active	
9	SPENA	Serial port data enable signal	
10	SPCK	SPI Serial Clock	
11	SPDA	SPI Serial Data Input/output	
12	DB0 (R0)	Data bus	
13	DB1 (R1)	Data bus	
14	DB2 (R2)	Data bus	
15	DB3 (R3)	Data bus	
16	DB4 (R4)	Data bus	
17	DB5 (R5)	Data bus	
18	DB6 (R6)	Data bus	
19	DB7 (R7)	Data bus	
20	DB8 (G0)	Data bus	
21	DB9 (G1)	Data bus	
22	DB10 (G2)	Data bus	
23	DB11 (G3)	Data bus	
24	DB12 (G4)	Data bus	
25	DB13 (G5)	Data bus	
26	DB14 (G6)	Data bus	
27	DB15 (G7)	Data bus	
28	DB16 (B0)	Data bus	
29	DB17 (B1)	Data bus	
30	DB18 (B2)	Data bus	
31	DB19 (B3)	Data bus	
32	DB20 (B4)	Data bus	
33	DB21 (B5)	Data bus	
34	DB22 (B6)	Data bus	
35	DB23 (B7)	Data bus	
36	HSYNC	Horizontal Synchronous Signal	
37	VSYNC	Vertical Synchronous Signal	
38	DOTCLK	Data Clock	
39	NC	No connect	
40	NC	No connect	

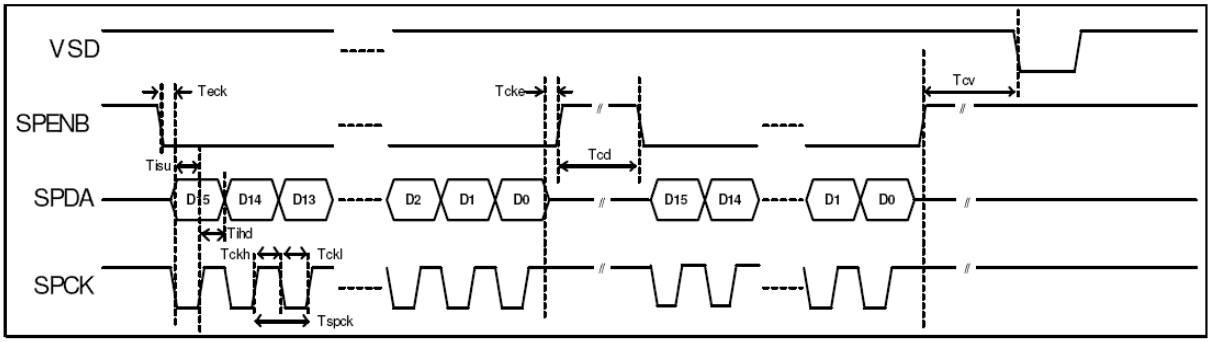
41	VDD	Power Supply	
42	VDD	Power Supply	
43	NC	No connect	
44	NC	No connect	
45	NC	No connect	
46	NC	No connect	
47	NC	No connect	
48	NC	No connect	
49	NC	No connect	
50	NC	No connect	
51	NC	No connect	
52	ENB	Data enabling signal	
53	GND	Ground	
54	GND	Ground	

9. AC Characteristics

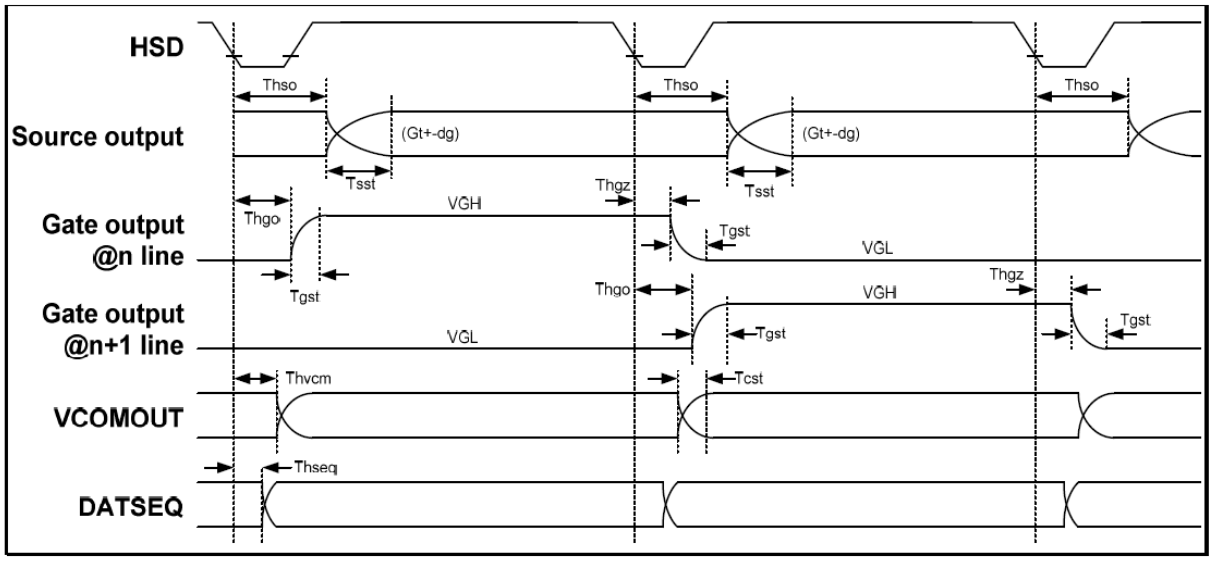
Clock and Data Input Timing Diagram



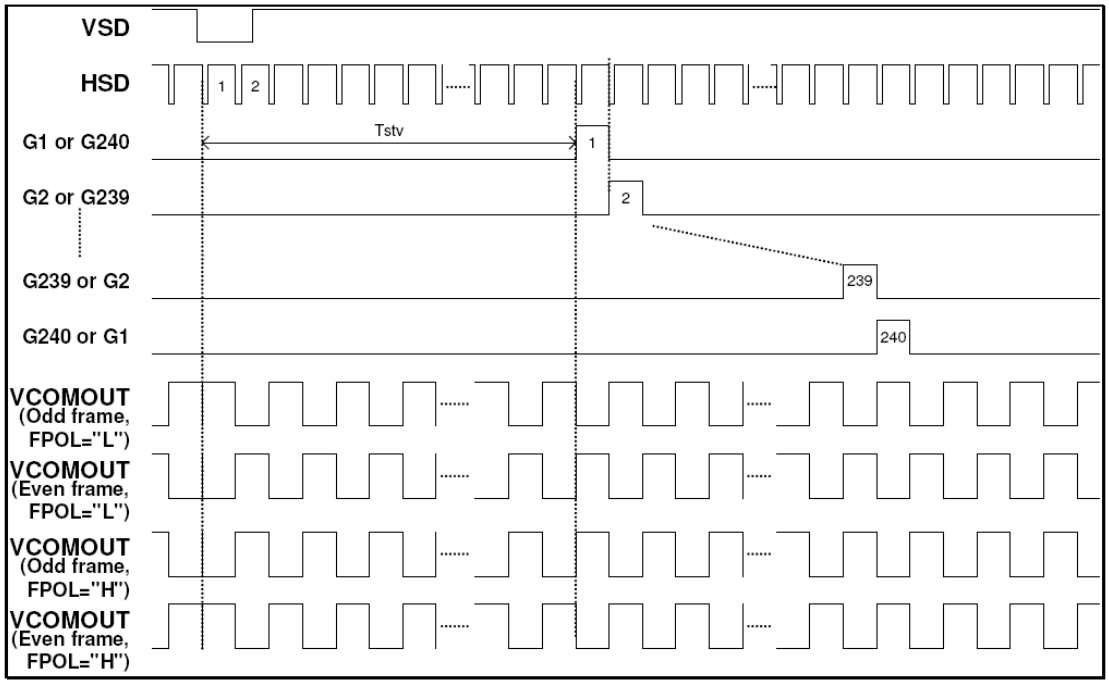
3-Wire Timing Diagram



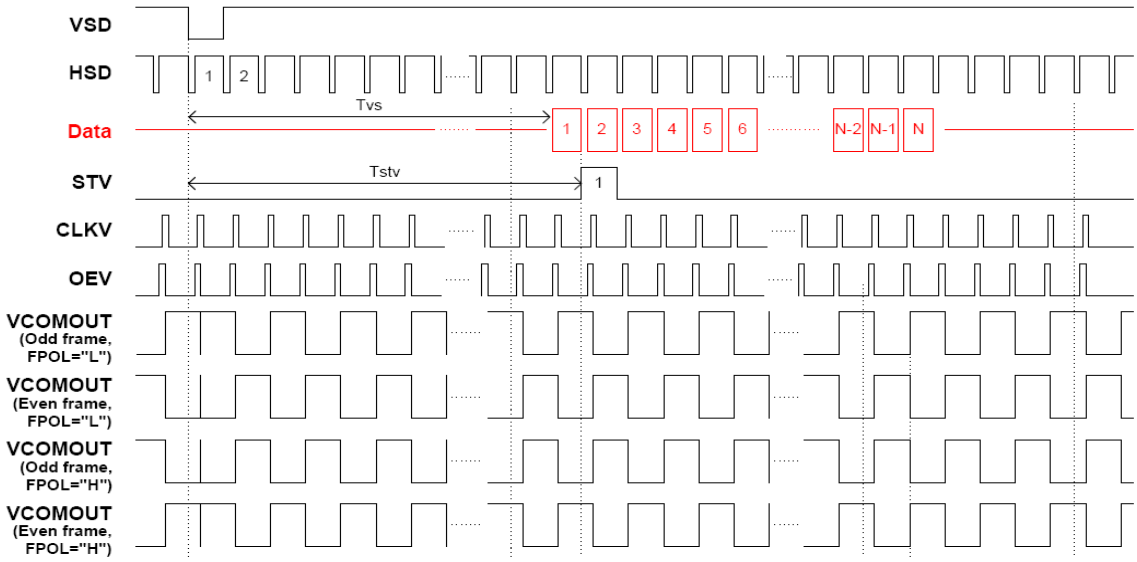
Source Driver Output Timing Diagram



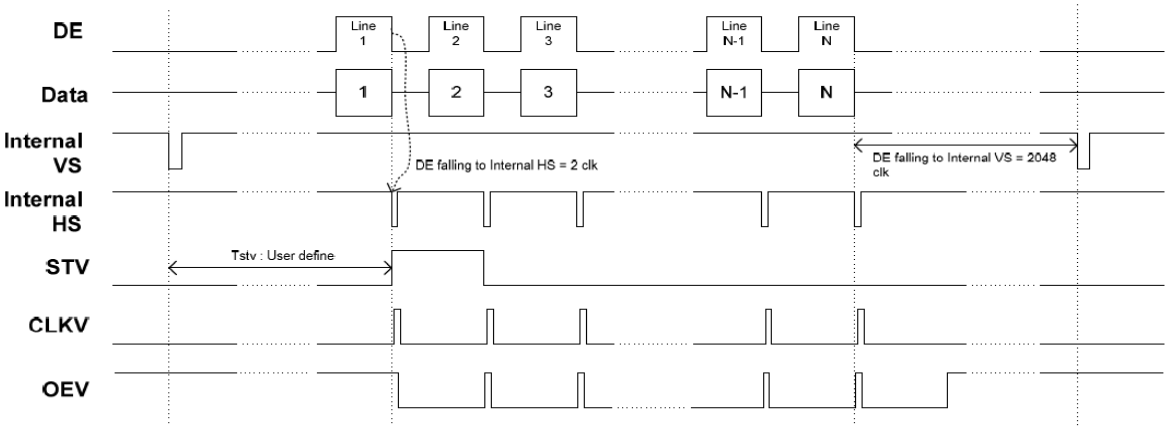
Gate Driver Output Timing Diagram



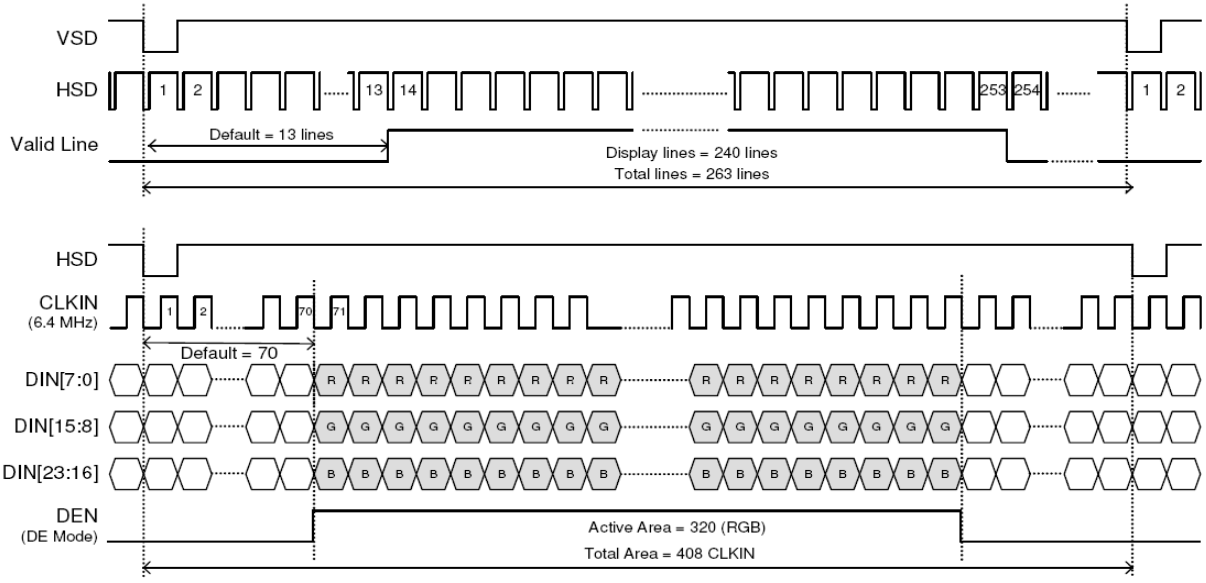
Vertical Timing Diagram (HV Mode)



Vertical Timing Diagram (DE Mode)



Input Data Timing (24 bit RGB mode for 960 x 240 @ SEL[3:0] = 1100b)



Test Condition: (VDD=VDDP=3.3V, VDDA=5.0V, GND=GNDA=GNDP=0V, TA= 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
System Operation Timing						
VDD power source slew time	T_{POR}			1000	us	From 0V to 90% VDD
RSTB active pulse width	T_{RSTB}	40			us	VDD = 3.3V
Input Output Timing						
CLKIN clock time	Tclk	-		35.7	ns	CLKIN = 28MHz
HSD to CLKIN	Thc	-	-	1	CLKIN	
HSD width	Thwh	1	-	-	CLKIN	
VSD width	Tvwh	1	-	-	Th	
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
Data set-up time	Tdsu	12	-	-	ns	DIN[23:0] to CLKIN
Data hold time	Tdhd	12	-	-	ns	DIN[23:0] to CLKIN
DEN setup time	Tesd	12	-		ns	DEN to CLKIN
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@CCIR601 / 8bit RGB HV mode Control by HDLY[6:0] setting Tvs = HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	12	20	28	Th	@CCIR656 NTSC mode Control by HDLY[6:0] setting Tvs = HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	17	25	33	Th	@CCIR656 PAL mode Control by HDLY[6:0] setting Tvs = HDLY[6:0]
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@24bit RGB HV mode Control by HDLY[6:0] setting Tvs = HDLY[6:0]
Source output stable time 1	Tst	-	25	30	us	96% final, CL=30pF, RL=2K
Gate output stable time	Tgst	-	500	1000	ns	96% final, CL=40pF
VCOMOUT output stable time	Tcst	-	4	8	us	96% final, CL=33nF, RL=100ohm
3-wire serial communication AC timing						
Serial clock	Tspck	320	-	-	ns	
SPCK pulse duty	Tscdut	40	50	60	%	
Serial data setup time	Tisu	120	-	-	ns	
Serial data hold time	Tihd	120	-	-	ns	
Serial clock high/low	Tssw	120	-	-	ns	
Chip select distinguish	Tcd	1	-	-	us	
SPENA to VSD	Tcv	1	-	-	us	

24 Bit RGB Mode (@ SEL[3:0] = 1100 or 1101)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	6.4		MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	Tclk	-	156		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time from HSD to VCOMOUT	Thvcm	-	30	-	CLKIN	
Time from HSD to DATSEQ	Thseq	-	20	-	CLKIN	
Time from HSD to Gate output n line	Thgz		5	-	CLKIN	
Time from HSD to Gate output n+1 line	Thgo		45	-	CLKIN	
Time that HSD to 1'st data input(NTSC)	Ths	40	70	255	CLKIN	DDLY =70, Offset = 0 (fixed)

10. Command Table

NT39016 3-Wire Control Register List (Default)

3-Wire Registers		Register Description		
D[15:10]	Name	Init.	R/W	Function Description
000000b	R00	07h	R/W	System control register
000001b	R01	00h	R/W	Timing Controller function register
000010b	R02	03h	R/W	Operation control register
000011b	R03	CCh	R/W	Input data Format control register
000100b	R04	46h	R/W	Source Timing delay control register
000101b	R05	0Dh	R/W	Gate Timing delay control register
000110b	R06	00h	R/W	Reserved
000111b	R07	00h	R/W	Internal function control register
001000b	R08	08h	R/W	RGB Contrast control register
001001b	R09	40h	R/W	RGB Brightness control register
001010b	R0A	88h	R/W	Hue / Saturation control register
001011b	R0B	88h	R/W	R / B Sub-Contrast control register
001100b	R0C	20h	R/W	R Sub-Brightness control register
001101b	R0D	20h	R/W	B Sub-Brightness control register
001110b	R0E	10h	R/W	VCOMDC Level Control Register
001111b	R0F	A4h	R/W	VCOMAC Level Control Register
010000b	R10	04h	R/W	VGAM2 level control register
010001b	R11	24h	R/W	VGAM3/4 level control register
010010b	R12	24h	R/W	VGAM5/6 level control register
011110b	R1E	00h	R/W	VCOMDC Trim function control register
100000b	R20	00h	R/W	Wide and narrow display mode control register

NT39016 3-Wire Register Bit Definition (Default)

3-Wire Control Register Bit Map								
Reg.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R00	PAT3	PAT2	PAT1	PAT0	PWMPDB	X	STBYB	RESETB
R01	X	X	X	SWD2	SWD1	SWD0	DITHB	CFTYP
R02	SKIPMOD	HDNC1	HDNC0	X	FPOL	VSET	UPDN	SHLR
R03	DENPOL	CLKPOL	HSDPOL	VSDPOL	SEL3	SEL2	SEL1	SEL0
R04	DDLY7	DDLY6	DDLY5	DDLY4	DDLY3	DDLY2	DDLY1	DDLY0
R05	X	HDLY6	HDLY5	HDLY4	HDLY3	HDLY2	HDLY1	HDLY0
R06	X	X	X	X	X	X	X	X
R07	FRAD1	FRAD0	INVSL1	INVSL0	PAL	PALM	-	AVGY
R08	X	X	X	CON4	CON3	CON2	CON1	CON0
R09	X	BRI6	BRI5	BRI4	BRI3	BRI2	BRI1	BRI0
R0A	HUE3	HUE2	HUE1	HUE0	SAT3	SAT2	SAT1	SAT0
R0B	SCONB1	SCONB0			SCONR1	SCONR0		
R0C	X	X	SBRIR5	SBRIR4	SBRIR3	SBRIR2	SBRIR1	SBRIR0
R0D	X	X	SBRIB5	SBRIB4	SBRIB3	SBRIB2	SBRIB1	SBRIB0
R0E	X	OTP_BYPS	VCDCSL5	VCDCSL4	VCDCSL3	VCDCSL2	VCDCSL1	VCDCSL0
R0F	VGLSL1	VGLSL0	VGHSL1	VGHSL0	VCACSL3	VCACSL2	VCACSL1	VCACSL0
R10	X	X	X	GAMEN	X	V2GAM2	V2GAM1	V2GAM0
R11	X	X	V4GAM2	V4GAM1	V4GAM0	V3GAM2	V3GAM1	V3GAM0
R12	X	X	V6GAM2	V6GAM1	V6GAM0	V5GAM2	V5GAM1	V5GAM0
R1E	TRMEN7	TRMEN6	TRMEN5	TRMEN4	TRMEN3	TRMEN2	TRMEN1	TRMEN0
R20	X	X	X	X	X	X	WNSEL1	WNSEL0

Note: Register function active at the falling edge of VSD except STBYB, RESETB register bits.

Registers require Vsync trigger table

DITHB	CFTYP	SKIPMOD	HDNC	FPOL	VSET	UPDN	SHLR	DDLY	HDLY	FRAD	INVSL
PAL	PALM	AVGY	CON	BRI	HUE	SAT	SCONB	SCONR	SBRIR	SBRIB	

11. Recommended Setting

TBD

12. Quality Assurance

12.1 Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

12.2 Standard for Quality Test

12.2.1 Sampling Plan:

ANSI / ASQC Z1.4-1993.

Single sampling, normal inspection.

12.2.2 Sampling Criteria:

Visual inspection: AQL 1.5%

Electrical functional: AQL 0.65%.

12.2.3 Reliability Test:

Detailed requirement refer to Reliability Test Specification.

12.3 Nonconforming Analysis & Disposition

12.3.1 Nonconforming analysis:

12.3.1.1 Customer should provide overall information of non-conforming sample for their complaints.

12.3.1.2 After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

12.3.1.3 If can not finish the analysis on time, customer will be notified with the progress status.

12.3.2 Disposition of nonconforming:

12.3.2.1 Non-conforming product over PPM level will be replaced.

12.3.2.2 The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

12.4 Agreement Items

Shall negotiate with customer if the following situation occurs:

12.4.1 There is any discrepancy in standard of quality assurance.

12.4.2 Additional requirement to be added in product specification.

12.4.3 Any other special problem.

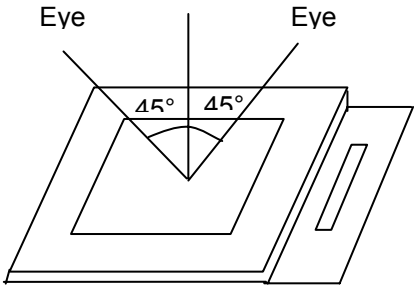
12.5 Standard of the Product Visual Inspection

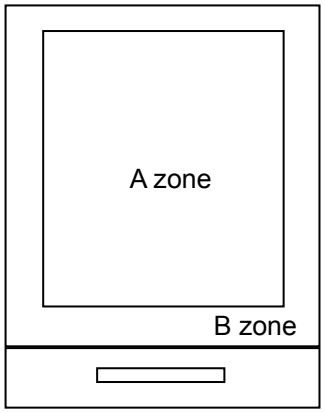
12.5.1 Appearance inspection:

12.5.1.1 The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

12.5.1.2 The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

12.5.1.3 Definition of area: A Zone: Active Area, B Zone: Viewing Area,



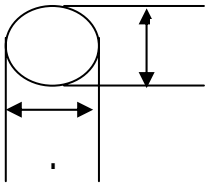


12.5.2 Basic principle:

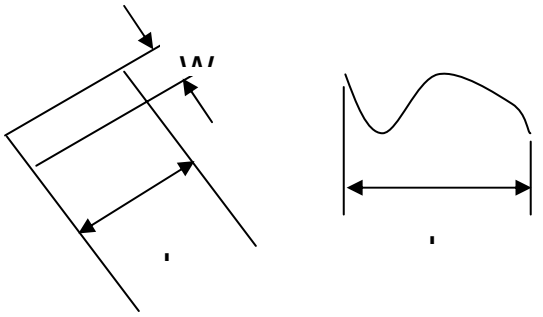
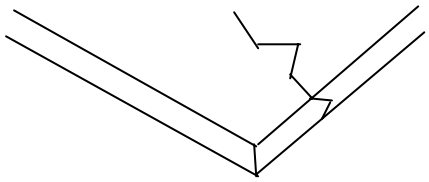
12.5.2.1 A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

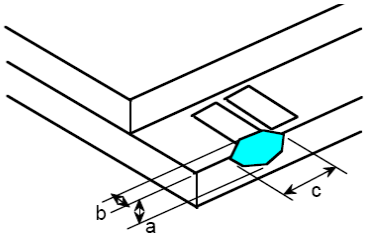
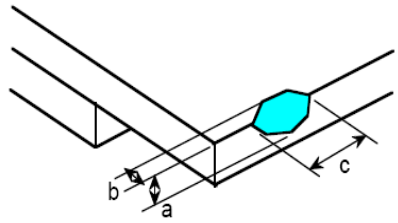
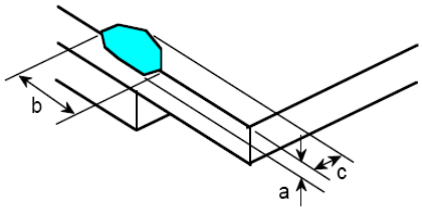
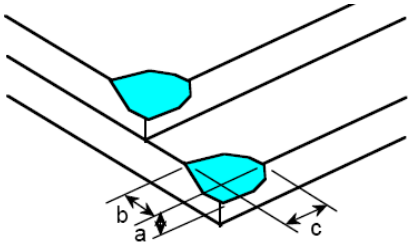
12.5.2.2 New item must be added on time when it is necessary.

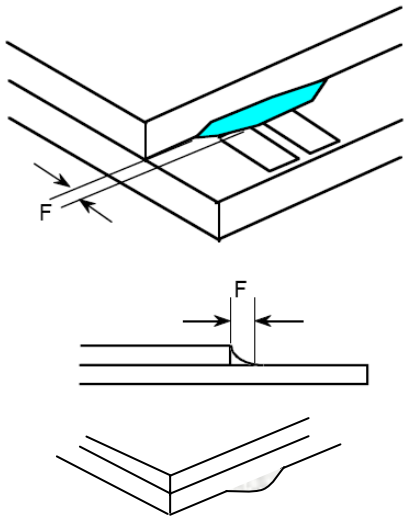
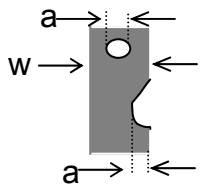
12.6 Inspection Specification

<table>
<tr><th>No.</th><th>Item</th><th>Criteria (Unit: mm)</th></tr>
<tr><td>01</td><td>Black / White spot
Foreign material
(Round type)
Pinholes
Stain
Particles inside cell.
(Minor defect)</td><td>


φ= (a + b) /2
<table>
<tr><th>Area / Size</th><th>Acc. Qty</th></tr>
<tr><td>φ≤0.10</td><td>Ignore</td></tr>
<tr><td>0.10<φ≤0.15</td><td>2</td></tr>
<tr><td>0.15<φ≤0.25</td><td>1</td></tr>
<tr><td>0.25<φ</td><td>0</td></tr>
<tr><td>Total</td><td>2 no include φ≤ 0.10</td></tr>
</table>
Distance between 2 defects should more than 3mm apart.
</td></tr>
</table>

<table>
<tr>
<td>02</td>
<td>Black and White line
Scratch
Foreign material
(Line type)
(Minor defect)</td>
<td>

<table>
<tr><th>Length</th><th>Width</th><th>Acc. Qty</th></tr>
<tr><td>/</td><td>W ≦ 0.03</td><td>Ignore</td></tr>
<tr><td>L ≦ 2.5</td><td>0.03 ＜ W ≦ 0.05</td><td>3</td></tr>
<tr><td>L ≦ 2.5</td><td>0.05 ＜ W ≦ 0.10</td><td>2</td></tr>
<tr><td>/</td><td>0.1 ＜ W</td><td>0</td></tr>
<tr><td colspan="2">Total</td><td>3</td></tr>
</table>
Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.
</td>
</tr>
<tr>
<td>03</td>
<td>Glass Crack
(Minor defect)</td>
<td>

Crack is potential to enlarge, any type is not allowed.
</td>
</tr>
</table>

<table>
<tr>
<td>04</td>
<td>Glass Chipping Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>3</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>05</td>
<td>Glass Chipping Rear of Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>06</td>
<td>Glass Chipping Except Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>07</td>
<td>Glass Corner Chipping:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c < 3.0, b< 3.0</td><td>Ignore</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
</table>

<table>
<tr><td>08</td><td>Glass Burr:
(Minor defect)
 
</td><td><table><tr><th>Length</th><th>Acc. Qty</th></tr><tr><td>F < 1.0</td><td>Ignore</td></tr></table>
Glass burr don’t affect assemble and module dimension.</td></tr>
<tr><td>09</td><td>FPC Defect:
(Minor defect)
 
</td><td>9.1 Dent, pinhole width a<w/3.
(w: circuitry width.)
9.2 Open circuit is unacceptable.
9.3 No oxidation, contamination and distortion.</td></tr>
<tr><td>10</td><td>Bubble on Polarizer
(Minor defect)</td><td><table><tr><th>Diameter</th><th>Acc. Qty</th></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>11</td><td>Dent on Polarizer
(Minor defect)</td><td><table><tr><th>Diameter</th><th>Acc. Qty</th></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>12</td><td>Bezel</td><td>12.1 No rust, distortion on the Bezel.
12.2 No visible fingerprints, stains or other contamination.</td></tr>
</table>

13	Touch Panel	D: Diameter W: width L: length 13.1 Spot: D<0.25 is acceptable 0.25≤D≤0.4 2dots are acceptable and the distance between defects should more than 10 mm. D>0.4 is unacceptable 13.2 Dent: D>0.40 is unacceptable 13.3 Scratch: W≤0.03, L≤10 is acceptable, 0.03<W≤0.10, L≤10 is acceptable Distance between 2 defects should more than 10 mm. W>0.10 is unacceptable.
14	PCB	14.1 No distortion or contamination on PCB terminals. 14.2 All components on PCB must same as documented on the BOM/component layout. 14.3 Follow IPC-A-600F.
15	Soldering	Follow IPC-A-610C standard
16	Electrical Defect (Major defect)	The below defects must be rejected. 16.1 Missing vertical / horizontal segment, 16.2 Abnormal Display. 16.3 No function or no display. 16.4 Current exceeds product specifications. 16.5 LCD viewing angle defect. 16.6 No Backlight. 16.7 Dark Backlight. 16.8 Touch Panel no function. 16.9 Dark Dot –one Allowed. 16.10 Bright Dot – one Allowed. Remark: 1. A pixel defect is acceptable if one color is none functional and causes a bright dot. The display may have one case where one color is out and cause a dark dot. 2. Bright dot caused by scratch and foreign object accords to item 1.

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

12.7 Classification of Defects

12.7.1 Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

12.7.2 Two minor defects are equal to one major in lot sampling inspection.

12.8 Identification/marking criteria

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

12.9 Packing

12.9.1 There should be no damage of the outside carton box, each packaging box should have one identical label.

12.9.2 Modules inside package box should have compliant mark.

12.9.3 All direct package materials shall offer ESD protection

13. Reliability Specification

No	Item	Condition	Quantity
1	High Temperature Operating	70℃, 96Hrs	5
2	Low Temperature Operating	-20℃, 96Hrs	5
3	High Humidity	50℃, 90%RH, 48Hrs	5
4	High Temperature Storage	80℃, 96Hrs	5
5	Low Temperature Storage	-30℃, 96Hrs	5
6	Thermal shock	-20℃, 30min~70℃, 30min, 10 cycles.	5

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

14. Precautions and Warranty

14.1 Safety

14.1.1 The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

14.1.2 Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

14.2 Handling

14.2.1 Reverse and use within ratings in order to keep performance and prevent damage.

14.2.2 Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

14.3 Storage

14.3.1 Do not store the LCD module beyond the specified temperature ranges.

14.4 Metal Pin (Apply to Products with Metal Pins)

14.3.2 Pins of LCD and Backlight

14.3.2.1 Solder tip can touch and press on the tip of Pin LEAD during the soldering

14.3.2.2 Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

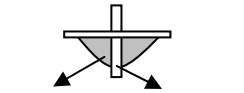
Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

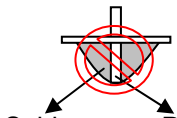
Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

14.3.2.3 Solder Wetting



Recommended



Not Recommended

14.3.3 Pins of EL

14.3.3.3 Solder tip can touch and press on the tip of EL leads during soldering.

14.3.3.4 No Solder Paste on the soldering pad on the motherboard is recommended.

14.3.3.5 Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270～290℃

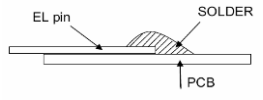
Typical Soldering Time: ≤2s

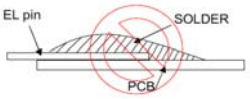
Minimum solder distance from EL lamp (body):2.0mm

14.3.3.6 No horizontal press on the EL leads during soldering.

14.3.3.7 180° bend EL leads three times is not allowed.

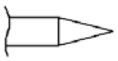
14.3.3.8 Solder Wetting

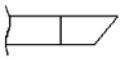




Recommended Not Recommended

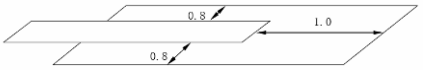
14.3.3.9 The type of the solder iron:





Recommended Not Recommended

14.3.3.10 Solder Pad



14.4 Operation

14.4.2 Do not drive LCD with DC voltage

14.4.3 Response time will increase below lower temperature

14.4.4 Display may change color with different temperature

14.4.5 Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.

14.5 Static Electricity

14.5.2 CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

14.5.3 The normal static prevention measures should be observed for work clothes and benches.

14.5.4 The module should be kept into anti-static bags or other containers resistant to static for storage.

14.6 Limited Warranty

14.6.1 Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.

14.6.2 If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used

.

15. Packaging

TBD

16. Outline Drawing